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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PAVEL N. LAPTEV

Appeal 2008-3500
Application 09/829,587
Technology Center 1700

Decided: August 5, 2008

Before ROMULO H. DELMENDO, LINDA M. GAUDETTE, and JEFFREY B. ROBERTSON, *Administrative Patent Judges*.

ROBERTSON, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) (2002) from the Examiner's final rejection of claims 1-21 and 43-51.[1] (Supplemental

[1] Claims 22-42 have been withdrawn from consideration. (Sixth Supplemental Appeal Brief filed Nov. 14, 2007, hereinafter "App. Br.," 2).

Examiner's Answer entered May 23, 2007, hereinafter "Ans"). We have jurisdiction pursuant to 35 U.S.C. § 6(b) (2002).

We REVERSE.

Appellant's claimed invention is directed to an apparatus for etching a surface of a wafer. (Spec. 2, ll. 1-6). The claimed combination includes a conduit for molecules of an inert gas, a first electrode, a second electrode, a wafer, and magnetic members. (Spec. 4, l. 5 – 5, l. 8). The first electrode, second electrode, and wafer are spaced from or displaced from each other. (Spec. 8, ll. 1-10 and 13, ll. 14-18). The first electrode is biased to a first negative voltage, and the second electrode is biased to a second negative voltage that is lower than the first voltage. (Spec. 4, ll. 11-15). Each voltage source may provide alternating voltage. *Id.* In another embodiment, the claimed combination includes an enclosure defined by the magnetic members and the first and second electrodes. (Spec. 4, ll. 6-10). The second electrode and the wafer provide a first capacitor of high impedance and the wafer and ions present in the enclosure provide a second capacitor of low impedance. (Spec. 4, l. 16 – 5, l. 4). The wafer and the electrode define a series relationship between the two capacitors. *Id.* Appellant states that an advantage of the apparatus is that it provides a current of low magnitude resulting in smooth and uniform etching of an insulating surface of the wafer without producing any pits. (Spec. 2, ll. 1-6, 14, l. 16 – 15, l. 5).

Claims 1, 7, 14, and 21, the independent claims on appeal, recite:

> 1. In combination for etching an insulating layer in a wafer to present a clean and fresh surface on the insulating layer for deposition, a conduit for molecules of an inert gas,
>
> a first electrode biased to a first voltage and spaced from the wafer,

a second electrode biased to a second voltage lower than the first voltage and spaced from the first electrode and the wafer and further spaced from the wafer than the first electrode,

magnetic members providing a magnetic field,

the first electrode and the magnetic members being disposed relative to each other and to the molecules of the inert gas for ionizing the molecules of the inert gas, and

the second electrode and the wafer being disposed relative to each other and to the ions of the inert gas, and the second electrode being constructed, to obtain a movement of the ions to the wafer at a low and controlled speed for an etching of the surface of the insulating layer by the ions at a low and controlled speed.

7. In combination for etching an insulating layer in a wafer to present a clean and fresh surface on the insulating layer for deposition,

an enclosure defined by magnetic members forming a magnetic field and by first and second electrodes spaced from each other and from the wafers and providing electrical fields,

a supply of molecules of an inert gas for introducing the molecules into the enclosure,

a first source of an alternating voltage for producing a direct negative voltage of a high magnitude on the first electrode for the creation of a first electrical field of a high magnitude in the enclosure,

a second source of an alternating voltage for producing a direct negative voltage of a low magnitude on the second electrode for the creation of a second electrical field of a low magnitude in the enclosure,

the molecules of the inert gas in the enclosure being ionized by the combination of the electrical and magnetic fields, and

the wafer being disposed relative to the second electrode and relative to the ions of the inert gas in the enclosure to receive an etching of a low magnitude on the surface of the insulating layer by the ions of the inert gas in the enclosure.

14. In combination for etching an insulating layer in a wafer disposed in an enclosure to present a clean and fresh surface on the insulating layer for deposition,

magnetic members defining a magnetic field in the enclosure,

a first source of an alternating voltage for providing a first electrical field of a high magnitude in the enclosure,

a first electrode forming a part of the enclosure and connected to the first source of voltage for providing a negative DC voltage of a relatively high magnitude at a first position in the enclosure,

a second source of an alternating voltage for providing a second electrical field of a low magnitude in the enclosure,

a second electrode forming a part of the enclosure and connected to the second source of the alternating voltage for providing a negative DC voltage of a relatively low magnitude at a second position displaced from the first position and the wafer but near the wafer,

a conduit for introducing molecules of an inert gas into the enclosure for ionization by the combination of the electrical and magnetic fields to produce ions of high density,

the second electrode and the wafer providing a first capacitor of a high impedance, and the wafer and the ions in the

enclosure providing a second capacitor of a low impedance, in a circuit to produce a current of a low magnitude for etching the surface of the insulating layer in the wafer.

21. In combination for etching an insulating layer in a wafer to present clean and fresh surfaces on the insulating layer for deposition,

an enclosure first and second electrodes disposed in the enclosure and displaced from each other and from the wafer for producing electrical fields in the enclosure, and

magnetic members disposed in the enclosure for producing a magnetic field in the enclosure in a direction transverse to the electrical field,

a first voltage source for producing a voltage of a high magnitude in the vicinity of the first electrode to obtain a production of a high electrical field in the enclosure,

a second voltage source for producing a voltage of a low magnitude in the vicinity of the second electrode to obtain a production of a low electrical field in the enclosure, and

a supply of molecules of an inert gas for introduction into the enclosure to cooperate with the first and second electrodes and the magnetic members in obtaining an ionization of the gas molecules in the enclosure by the electrical and magnetic fields in the enclosure and in obtaining a movement of the ions in the enclosure to the insulating layer in the wafer at a speed to obtain a smooth and uniform etching of the surface of the insulating layer at a low rate without any pits in the surface of the insulating layer.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Mountsier	5,810,933	Sep. 22, 1998
Koshimizu	5,987,687	Nov. 9, 1999

There are three rejections before us on Appeal: (1) the rejection of claims 1-4, 7-9, 11, 14-16, 19-21, 43-47, and 51 under 35 U.S.C. § 102(b) as being anticipated by Koshimizu and demonstrated by Mountsier; (2) the rejection of claims 5, 6, 10, 12, 13, 17, 18, 20, 48, and 49 under 35 U.S.C. § 103(a) as being unpatentable over Koshimizu in view of Mountsier; and (3) the rejection of claims 1-21 and 43-51 under 35 U.S.C. § 103(a) as being unpatentable over Appellant's own admitted prior art in view of Mountsier.

Appellant's principal dispute is with the Examiner's finding that the prior art discloses the second electrode is "spaced from" or "displaced from" the wafer as presently claimed. The Examiner found that as evidenced by Mountsier, Koshimizu inherently discloses a space between the wafer and the second electrode. (Ans. 6). Moreover, the Examiner determined that in view of Appellant's admission that the only difference between the prior art and the present combination is the separation between the second electrode and the wafer, it would have been obvious to replace the wafer support platform of Appellant's admitted prior art with Mountsier's wafer support platform. (Ans. 8). The Examiner found that Mountsier's wafer support platform would produce the claimed capacitors and the required series relationship between them. (Ans. 7 and 8).

Appellant contends that the Examiner's finding that all wafers and electrodes have a gap, does not mean that the electrode and wafer are completely separated, arguing that Mountsier demonstrates that the wafer and the electrode are not separated. (App. Br. 10 and 11). Appellant argues that the language of "spaced from" or "displaced from" together with the specification language of "separation" means that the wafer does not possess any contact points with the two electrodes. (App. Br. 11). In addition,

Appellant contends that for the second electrode and the wafer to form a capacitor, there has to be complete separation between the electrode and the wafer. (App. Br. 13). Otherwise, Appellant argues, the electrode and the wafer will be electrically connected, forming a conductor, and not a capacitor. *Id*. Appellant also argues that Mountsier does not disclose a series relationship between two capacitors, because Mountsier fails to disclose a second insulator. (App. Br. 14 and 15).

The Examiner responds that Mountsier's Figures 5 and 6 show that spacing exists between wafers and surfaces supporting them, including electrode surfaces arguing that Mountsier is a demonstration of the inherency in any structure that supports a wafer. (Ans. 9). Further, the Examiner contends that the claimed invention does not specify the word "separation" in any of the finally rejected claims and that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. (Ans. 10 and 11). The Examiner also argues that Mountsier's apparatus would have a capacitance between the wafer and ceramic disk in order for the wafer to be mounted using electrostatic force. (Ans. 12).

ISSUE

Based on the contentions of the Examiner and the Appellant, the issue presented is: Has Appellant shown error in the Examiner's determination that the prior art discloses a space between the electrodes and the wafer?

We answer this question in the affirmative.

FINDINGS OF FACT

The record supports the following Findings of Fact (FF) by a preponderance of the evidence.

1. Figure 1 of Appellant's Specification is reproduced below:

FIG. 1

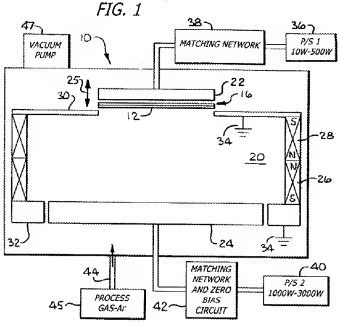

Figure 1 depicts an apparatus for etching a surface of a wafer. Figure 1 includes a first electrode (24), a second electrode (22) and a wafer (16). (Spec. 8, ll. 1-10).

2. Appellant's Specification states:

> The electrode 22 is disposed in a contiguous and substantially paralle1 relationship to the wafer 16 and is movable in position toward or away from the wafer, as indicated by a double-headed arrow 25. The spacing between the wafer 16 and the electrode 22 may illustratively be in the order of 0.1 - 2mm. (Spec. 8, ll. 4-7).

3. Figure 4a of Appellant's Specification is reproduced below:

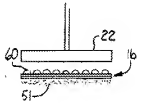

Fig. 4a

Figure 4a shows an enlarged fragmentary elevational schematic view showing the disposition of particular components in Figure 1. (Spec. 6, ll. 3-4).

4. Appellant's Specification states:

> Applicant's assignee of record in this application has previously sold one (1) unit of apparatus with features similar to the apparatus shown in Figure 1. This unit may have been sold more than one (1) year prior to the date of this application. However, there is one significant difference between the apparatus 10 constituting the preferred embodiment of the invention and the unit previously sold by applicant's assignee. The significant difference is that the wafer 16 engaged the electrode 22 in the one (1) unit sold prior to the date of this application. The circuit equivalent of this arrangement is shown in Figure 5b and is indicated prior art in that Figure. As previously indicated, the wafer 16 is separated from the electrode 22 in the preferred embodiment 10 of this invention. (Spec. 12, ll. 1-9).

5. Figure 1 of Koshimizu is reproduced below:

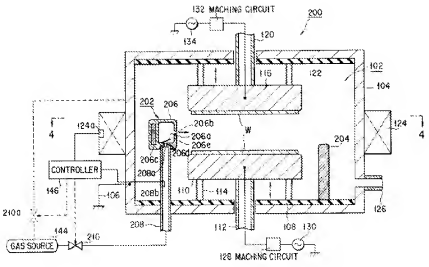

Fig. 1

Figure 1 is an etching apparatus according to the Koshimizu's invention. Figure 1 includes electrodes (110) and (116) and wafers (W). (Col. 4, ll. 8-21).

6. Koshimizu states:

> A second susceptor **116** which constitutes an upper electrode and can fix a wafer **W** thereon is opposed to the mount surface of the first susceptor **110** with a predetermined space therebetween. (Col. 4, ll. 8-11).

7. Figure 5 of Mountsier is reproduced below:

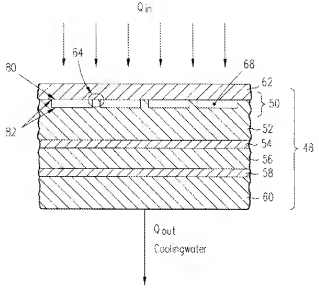

FIG. 5

Figure 5 depicts a wafer cooling device according to Mountsier's invention. Wafer (62) is mounted to ceramic disk (52) forming interface (50) with gaps (68). (Col. 5, ll. 8-20).

8. Figure 6 of Mountsier is reproduced below:

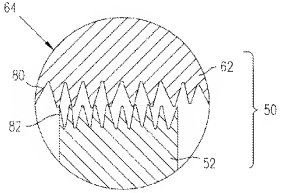

FIG. 6

Figure 6 depicts the interface (50) between the wafer (62) and its support (ceramic disk 52) shown in Figure 5 with contact surfaces (80) and (82). (Col. 5, ll. 21-27).

9. Mountsier states:

> As shown in FIG. **6**, at wafer-WCD interface **50**, only microscopic points of contact (exaggerated in illustration) between wafer **62** and ceramic disc **52** exist since the contact surface **80** of wafer **62** and the contact surface **82** of ceramic disk **52** are not perfectly smooth. (Col. 5, ll. 24-28).

10. Figure 6 of Mountsier shows that there are points of contact between the wafer and the support such that the electrode is not spaced from or displaced from the wafer as presently claimed.

11. Alleged gaps 68 and 80/82 are part of the same interface between the wafer (62) and the support (52). (Mountsier, Figs. 5 and 6).

12. The interface (50) does not give rise to two capacitors arranged in a series relationship as presently claimed.

PRINCIPLES OF LAW

During prosecution, claims are given the broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004). Claims will be given their plain meaning unless their plain meaning is inconsistent with the Specification. *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior

art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987), *cert. denied*, 484 U.S. 827 (1987). Analysis of whether a claim is patentable over the prior art under 35 U.S.C. § 102 begins with a determination of the scope of the claim. We determine the scope of the claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction in light of the Specification as it would be interpreted by one of ordinary skill in the art. *Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d at 1364.

In construing claims "we search for the ordinary and customary meaning of a claim term to a person of ordinary skill in the art. We determine this meaning by looking first at intrinsic evidence such as surrounding claim language, the specification, the prosecution history, and also at extrinsic evidence, which may include expert testimony and dictionaries." *L.B. Plastics, Inc. v. American Home Products Inc.,* 499 F.3d 1303, 1308 (Fed. Cir. 2007) (citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314-19 (Fed. Cir. 2005) (en banc)). The properly interpreted claim must then be compared with the prior art.

"Section 103 forbids issuance of a patent when the 'differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.' " *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1734 (2007).

ANALYSIS

We begin by interpreting the recitations in the claims that the wafer and the electrodes are either "spaced from" (claims 1 and 7) or "displaced

from" (claims 14 and 21) each other.[2] As acknowledged by Appellant, the Specification does not provide a clear definition of "spaced." (Reply Brief filed Sep. 13, 2006, hereinafter "Reply Br.," 9 and 10). However, Appellant contends that the plain meaning of the word "spaced" is equivalent to "separated," which is consistent with the Specification. (App. Br. 10 and 11). Appellant also cites a dictionary definition of "spaced" to support their position. (Reply Br. 10). The Examiner argues that this interpretation would require reading limitations from the Specification into the claims. (Ans. 11).

Reading the claims in light of the Specification, it is clear that the term "spaced from" requires complete separation between the second electrode and wafer. The Specification states that the second electrode is "substantially parallel" to the wafer and that the spacing between the wafer and the electrode is "in the order of 0.1 to 2 mm." (FF 2). In addition, Figures 1 and 4a show that there is complete separation between second electrode (22) and wafer (16). (FF 1 and 3). Further, Appellant indicates that the difference between the prior art and a preferred embodiment of the present invention is the separation between the wafer and second electrode. (FF 4). Thus, contrary to the Examiner's argument that Appellant's interpretation reads limitations from the Specification into the claims, to interpret the claims as not requiring complete separation between the wafer and the second electrode would be inconsistent with the Specification. *Zletz*,

[2] We note that both Appellant and the Examiner focus their arguments on the "spaced from" language of claims 1 and 7, rather then the "displaced from" language in claims 14 and 21. For the purposes of our discussion, we will do the same, with the understanding that our comments apply equally to the "displaced from" language in claims 14 and 21.

893 F.2d at 321. In addition, our interpretation is consistent with the dictionary definition provided by Appellant that "spaced" means "to organize or arrange with spaces in between" or "to separate or keep apart." (Reply Br. 10).

Regarding the rejection of claims 1-4, 7-9, 11, 14-16, 19-21, 43-47, and 51 under 35 U.S.C. § 102(b) as being anticipated by Koshimizu and demonstrated by Mountsier, Koshimizu requires that the wafer is fixed to the upper electrode. (FF 5 and 6). However, the Examiner relies on Figures 5 and 6 of Mountsier to demonstrate that the electrodes and the wafers disclosed in Koshimizu are "spaced from" each other. (Ans. 6 and 7). In light of the above claim interpretation, Figures 5 and 6 of Mountsier do not demonstrate the claimed relationships between the electrode and the wafer. Specifically, Figure 6 of Mountsier shows the interface between the wafer (62) and its support (ceramic disk 52). (FF 8). Figure 6 shows that there are points of contact between the wafer and the support such that the electrode is not spaced from the wafer as presently claimed. (FF 8-10). Indeed, Mountsier specifically discloses that there are microscopic points of contact between the wafer/support interface. (FF 9). Thus, Koshimizu as evidenced by Mountsier, does not anticipate the present claims.

Regarding the rejection of claims 1-21 and 43-51 under 35 U.S.C. § 103(a) as being unpatentable over Appellant's own admitted prior art in view of Mountsier, the present claims are not rendered obvious by Appellant's admitted prior art in view of Mountsier. As discussed above, Figures 5 and 6 of Mountsier fail to teach complete separation between the wafer and the electrode. Therefore, even if Appellant's admitted prior art is

combined with Mountsier, the presently claimed combination does not result.

In addition, the Examiner found that Mountsier teaches a wafer support platform that provides a series relationship between two capacitors, one having a high capacity impedance and the other having a low capacity impedance. (Ans. 8). The Examiner also found that because the wafer support in Mountsier is made of an electrically insulating material, capacitance across the stated points is established. (Ans. 8). The Examiner found that Mountsier teaches a series relationship between two capacitors, where one dielectric gap corresponds to reference number 68 in Figure 5 and the other dielectric gap corresponds to reference number 80/82 in Figure 6. (Ans. 8). We agree with Appellant that Mountsier does not disclose two capacitors in a series relationship, but the formation of one capacitor. (App. Br. 14 and 15). We also agree with Appellant that the alleged dielectric gaps 68 and 80/82 are part of an insulator located between two electrodes. (App. Br. 15). Figure 6 shows a blown up cross section of the wafer support interface of Figure 5. (FF 8). Thus, alleged gaps 68 and 80/82 are part of the same interface between the wafer (62) and the support (52). (FF 11). As a result, this interface does not give rise to two capacitors arranged in a series relationship as presently claimed. (*See* App. Br. 15; FF 12). Therefore, the present claims are not rendered obvious by Mountsier.

Regarding the rejection of claims 5, 6, 10, 12, 13, 17, 18, 20, and 48, because we find that independent claims 1, 7, 14, and 21 are not anticipated or obvious in view of the cited prior art as discussed above, the dependent claims are also not anticipated or obvious over the prior art of record.

CONCLUSION

For the foregoing reasons, Appellant has shown reversible error on the part of the Examiner.

ORDER

The decision of the Examiner rejecting claims 1-4, 7-9, 11, 14-16, 19-21, 43-47, and 51 under 35 U.S.C. § 102(b) as being anticipated by Koshimizu and demonstrated by Mountsier is reversed. The decisions of the Examiner rejecting claims 5, 6, 10, 12, 13, 17, 18, 20, 48, and 49 under 35 U.S.C. § 103(a) as being unpatentable over Koshimizu in view of Mountsier, and claims 1-21 and 43-51 under 35 U.S.C. § 103(a) as being unpatentable over Appellant's own admitted prior art in view of Mountsier are also reversed.

REVERSED

PL initial:
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